REMARKS

In the Office Action mailed December 4, 2003, Claims 1-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over applicant's admitted prior art in view of US Patent 6,643,714 to Chrysanthakopoulos (referred to herein as the "'714 patent.") Claim 1 in the present application is presented here:

1. In a serial bus module having a plurality of link devices, a method for presenting the plurality of link devices as separate nodes comprising:
   a) creating an individual configuration ROM image for each link device; and
   b) presenting said configuration ROM image for each said link device.

A. Applicant respectfully submits that Examiner has mischaracterized Applicant's admitted prior art.

In the Office action mailed 12/3/03, Examiner stated that Applicant's admitted prior art teaches "creating a configuration ROM image for each link device; and presenting said configuration ROM image for each said link device." Examiner cites FIG. 2 and page 4, lines 9-20 of the present application.

1. Applicant respectfully submits that FIG. 2 (prior art) only shows that a separate configuration ROM is created for each link device. However, FIG. 2 does not show these separate configuration ROM images being presented individually. FIG. 2 is included in the application to illustrate the problem solved by Applicant's invention.

2. Applicant respectfully submits that Page 4, lines 9-20 of the present application do not teach presenting individual configuration ROM images. Page 4, lines 9-20 are reproduced below for the Examiner's convenience:

> According to the prior art, a serial bus module may include one or more nodes. For example, FIG 2 illustrates a typical module device 1 having first and second nodes 2a, 2b Nodes 2a, 2b include respective link layer services (LINK) 3a, 3b and physical layer services (PHY) 4a, 4b. Each link device 3a, 3b includes a respective global unique identifier (GUID) 5a, 5b to identify each node device 2a, 2b.
>
> Presently, the configuration ROM described above is managed by software operating at the transaction layer 6 in module 1. **However, current transaction layer implementations which support multiple link devices (such as depicted in FIG. 2) present a single configuration ROM image 7 for both link devices.** (emphasis added)

Thus, Applicant respectfully asserts that the admitted prior art of presenting a single configuration ROM image 7 for both link devices is fundamentally different from Examiner's characterization that applicant's admitted prior art teaches creating a configuration ROM image for each link device; and presenting said configuration ROM image for **each** said link device.

B. Applicant respectfully submits that Examiner has mischaracterized cited prior art Chrysanthakopoulos, and that presenting a separate configuration ROM image for each link device is not taught by Chrysanthakopoulos.

1. Applicant respectfully asserts that the cited portion of Chrysanthakopoulos discusses nodes, not link devices. Examiner cited FIG. 3 and col. 1, lines 40-44 in Chrysanthakopoulos.

a. FIG. 3 is a schematic block diagram illustrating an exemplary logical node architecture for use in communicating via a serial bus (col 2, lines 52-54). FIG. 3 is discussed at col. 5, lines 24-31, reproduced below for the Examiner's convenience:

> The logical organization of nodes and units is further illustrated in FIG. 3, where a module 301 comprising a plurality of nodes 303-305 is shown. A module is a physical device, coupled to a serial bus 312, having one or more nodes. Each of the nodes may comprise one or more units 307-310. The implementation and operation of the nodes is well known in the art.

This language in Chrysanthakopoulos does not disclose, teach, nor otherwise suggest creating a configuration ROM image for each link device nor presenting said configuration ROM image for each link device. Chrysanthakopoulos does not even disclose, teach, nor otherwise suggest link devices, nor configuration ROM images.

PAGE 7/9 * RCVD AT 3/4/2004 8:47:35 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:7755869550 * DURATION (mm-ss):02-54

b. Col.1, lines 40-44 likewise do not disclose, teach, nor otherwise suggest an individual configuration ROM image for each link device, as asserted by Examiner. Col. 1, lines 40-44, are presented below for the Examiner's convenience.

> Nodes are logical entities, each with a unique address. In a preferred implementation, each node provides a so-called configuration ROM (read-only memory)-hereinafter referred to as configuration memory-and a standardized set of control registers that can be accessed by software residing within the computer system

Examiner's attention is directed to the text just above this passage of Chrysanthakopoulos, at col. 1, lines 32-40, also reproduced for the Examiner's convenience:

> A typical serial bus having an IEEE 1394 standard architecture is comprised of a multiplicity of nodes that are interconnected via point-to-point links, such as cables, that each connect a single node of the serial bus to another node of the serial bus. The nodes themselves are addressable entities which can be independently reset and identified. Nodes are associated with respective components of a computer system and serve as interfaces between the components and communications links

This text supports Applicant's arguments in earlier responses that nodes, in IEEE 1394 terminology, are not link devices as described in IEEE 1394 terminology. Directing attention back to Applicant's FIG. 2, a link device (3a) is contained within a node (2a).

Applicant asserts that because the Chrysanthakopoulos doesn't even address the problem referred to in the background of the present application, and merely describes this aspect of the existing prior art in a more basic form, the Chrysanthakapoulos, when viewed in light of Applicant's admitted prior art, does not make obvious the present invention.

The above analysis also applies to Claims 5, 7, and 9, as these claims in the present application contain similar limitations as recited in Claim 1. As remaining claims are dependent from claims 1, 5, 7 and 9, applicant respectfully asserts that these claims also are patentable as they contain the same limitations as their respective parent claims.

PAGE 8/9 * RCVD AT 3/4/2004 8:47:35 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:7755869550 * DURATION (mm-ss):02-54

For the above reasons, Applicant respectfully submits that the 35 USC § 103 rejections have been traversed. Applicant respectfully requests that all the claims be allowed over the prior art.

On the basis of the above remarks, early consideration of this application and early allowance are respectfully requested.

INVITATION TO TELEPHONE CONFERENCE

Examiner is invited to call the undersigned attorney if the Examiner feels any remaining issues can be resolved by phone.

Respectfully submitted,
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PAGE 9/9 * RCVD AT 3/4/2004 8:47:35 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:7755869550 * DURATION (mm-ss):02-54